A Bidirectional Snubber Less Soft-switched High Frequency Link DC/AC Converter

Anirban Pal and Kaushik Basu
Department of Electrical Engineering,
Indian Institute of Science, Bangalore- 560012, India
Email: palanirban@ee.iisc.ernet.in, basu@ee.iisc.ernet.in

***Abstract*—This paper presents two novel modulation schemes for a bidirectional single phase inverter with a high frequency link. The topology with the proposed modulation scheme can be used for the grid integration of renewable energy sources like photovoltaic and fuel cell, energy storage system, hybrid and electrical vehicle, vehicle to grid (V2G) integration, uninterruptible power supply (UPS) system. The use of high frequency transformer results in reduction of cost with improved power density. The proposed modulation strategies of the converter achieve soft-switching for both direction of power flow. During DC to AC power flow, modulation is done in the DC side with zero voltage switching (ZVS) of the DC side switches and the AC side switches are line frequency switched. For AC to DC power flow, zero current switching (ZCS) of AC side switches and zero voltage switching (ZVS) of DC side switches are achieved. A detailed analysis of operation of the proposed converter is presented in the paper. Key simulation results are shown to demonstrate the effectiveness of the proposed topology.**

***Index Terms*- SPWM inverter, cyclo-converter, high frequency transformer (HFT), AC/DC converter, DC/AC converter, zero voltage switching (ZVS), zero current switching (ZCS), bidirectional power flow.**

I. Introduction

High frequency link based inverter topologies are becoming attractive solution for modern power electronic applications like grid integration of renewable and alternative energy sources (photovoltaic, wind, fuel cell) [1]–[3], energy storage system, hybrid and electric vehicle [4], [5], vehicle to grid integration, uninterruptible power supplies (UPS) [6], compact power module in naval and space applications. The conventional energy management system uses line frequency transformer to achieve required voltage magnification and provide galvanic isolation to ensure safety. But the line frequency transformer increases the system volume and overall cost. The low volume, weight and low cost high frequency topologies with improved power density and efficiency are replacing the conventional line frequency solutions.

The single phase single stage high frequency link (HFL) inverter topologies discussed in literature generally have a high frequency inverter (H-bridge) in the DC side of the high frequency transformer (HFT). In one of such topologies in the AC side of the HFT [7]–[9], two back to back H-bridge are used to convert the high frequency square wave to desired frequency and magnitude AC. In some other topologies [10]–[12] a cyclo-converter is used in the AC side to get the line frequency AC. Several modulation strategies with additional snubber circuit are discussed in literature to achieve soft switching of HFL inverters. A source based commutation technique is used in [13] to eliminate additional snubber circuit. A DC side side push-pull based soft-switched HFL inverter is proposed in [14] which uses leakage energy of HFT to achieve soft switching. In [4], [15], [16] current fed isolated soft-switched HFL DC-DC topologies are discussed. But here additional inductors are used in series with HFT to limit the transformer current during soft switching which causes additional voltage drop across the inductors.

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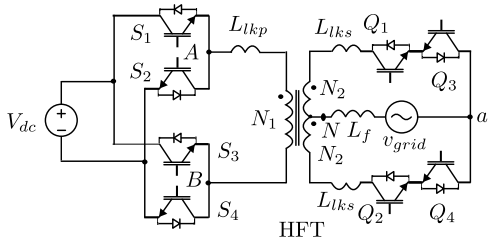


Fig. 1: Single phase cyclo-converter based HFL topology for which novel modulation strategies are proposed

In [17] modulation strategy of a single phase bidirectional soft-switched HFL topology with AC side cyclo-converter is proposed. For DC to AC side power flow the modulation is done in AC side which leads to high frequency switching of both the DC and AC side converters causing higher switching loss. The cyclo-converter has four AC switches in a H-bridge structure causing higher conduction loss compared to a centre tap structure (see Fig. 1) with two AC switches. In addition, the soft-switching is shown only for DC to AC active power flow.

This paper presents two novel modulation strategies of a single phase, single stage, high frequency link (HFL) inverter shown in Fig. 1 for both direction of power flow with out using any additional snubber circuits. AC side modulation of the converter with out using any additional snubber like in [17] leads to hard switching of the converter. The proposed modulation schemes have following advantages- (i) DC to AC side power flow- (a) modulation is done in DC side, AC side switches are line frequency switched, (b) soft-switching (zero voltage switching) of dc side converter is achieved using leakage inductance of

HFT and device parasitic capacitances; (ii) AC to DC side power flow- (a) zero current turn ON and turn OFF of AC side switches, (b) zero voltage turn ON and OFF of DC side switches, (c) AC side switches are switched at high frequency for half of the line frequency cycle, (d) no additional series inductor with HFT is required to limit the transformer current shoot up during commutation as the current is naturally commutated by the body diodes of AC switches; (iii) reduced size and cost due to HFT.

The paper is organized as follows. Section II presents modulation strategy and soft-switching technique for both direction of power flow. Key simulation results are presented in section III.

II. Steady state operation and analysis

In this section the steady state operation of the converter is discussed for bidirectional power flow. The switching scheme is different for the two power flow directions. The reference (v_{ref}) to generate PWM voltage across aN is in phase (for DC to AC active power flow) and in out of phase (for AC to DC active power flow) with the grid current i_S where the grid current is assumed to be ripple free sinusoidal current source at the line frequency. The line frequency current i_S is considered as constant with in a switching frequency cycle $\frac{1}{2T_S}$ where T_S is the carrier frequency. The device parasitic capacitance and transformer leakage inductance are used to achieve soft-switching for both the direction of power flow. Here, the commutation process means the change over of current from one set of switches to other set of similar switches.

A. Active power flow direction: AC to DC

The modulation scheme for AC to DC active power flow is shown in Fig. 2. During the positive half cycle of the line current i_S, gating signals are applied to Q_1 and Q_2 and the devices Q_3, Q_4 are kept OFF as shown in Fig. 2b. The gating signal of Q_2 is same as of Q_1 except 180° phase shift between the two (Fig. 2b). The reference voltage v_{ref} is the rectified version of the modulation waveform used to generate PWM voltage across aN. The reference voltage can be expressed as-

$$v_{ref} = 0.5 + 0.5\frac{N_1 V_m}{N_2 V_{dc}}|\sin(2\pi f t)| \tag{1}$$

where V_m is the peak value of the sinusoidal AC input and V_{dc} is the DC bus voltage. f is line frequency and $N_{1,2}$ are primary and secondary turns of the transformer respectively. The turn ON times of S_1 and S_4 are synchronised with the turn ON of Q_1 and the turn OFF is synchronised with the turn OFF of Q_2. Similarly, S_2 and S_3 are gated ON with Q_2 and turned OFF with Q_1. During the negative cycle, switching strategy is similar except the gating signals are applied to Q_3 and Q_4 and the devices Q_1, Q_2 are kept OFF. The commutation process in one half of the high frequency switching cycle $\frac{1}{2T_S}$ is explained in details when grid current is positive. In rest high frequency half cycle, the shown intervals are repeated with other symmetrical switches. Fig. 3 and Fig. 4 shows the commutation process and voltage, current wave forms along with device gating signals for active power flow from AC to DC side.

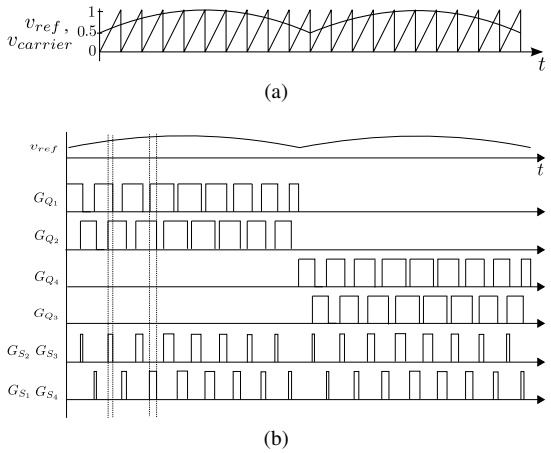


Fig. 2: Modulation strategy for AC to DC active power flow- (a) carrier and reference waveform (b) switching scheme in a line frequency cycle.

1) Mode 1: (Fig. 3a, $t_0 < t < t_1$): In this interval the switch Q_1 and the the body diode of Q_3 are conducting. In the DC side the body diodes of S_2 and S_3 are in conduction and transferring the active power from AC to DC. The AC and DC side currents are given as: $i_{S_T} = i_S$ and $i_p = \frac{N_2}{N_1} i_S$ respectively. N_1 and N_2 are the DC and AC side transformer turns ratio respectively. The device S_1 and S_4 are blocking V_{dc}. The voltage across the devices Q_2 and Q_4 is $(\frac{2N_1}{N_2} \cdot V_{dc})$.

2) Mode 2: (Fig. 3b, $t_1 < t < t_2$): At the instant t_1 the switches Q_2, S_2 and S_3 are gated ON. The turning ON of Q_2 forward biases the anti-parallel body diode of Q_4 and it starts conducting. The current through Q_1 starts falling linearly. The circuit equations are given as-

$$i_p = \frac{N_2}{N_1}(i_{S_T} - i_{S_B}) \tag{2}$$

$$i_S = i_{S_T} + i_{S_B} \tag{3}$$

$$i_{S_B} = \frac{V_{dc}}{L_{lks}} \cdot \frac{N_2}{N_1} \cdot (t - t_1) \tag{4}$$

$$i_{S_T} = i_S - \frac{V_{dc}}{L_{lks}} \cdot \frac{N_2}{N_1} \cdot (t - t_1) \tag{5}$$

$$i_p = \frac{N_2}{N_1} i_S - \frac{2 \cdot V_{dc}}{L_{lks}} \cdot \left(\frac{N_2}{N_1}\right)^2 \cdot (t - t_1) \tag{6}$$

where L_{lks} is the transformer leakage inductance seen from AC side. The zero current (ZC) turn on of Q_2 is achieved as in Fig.4. As the body diodes of S_2 and S_3 are conducting, the turn on of S_2 and S_3 is zero voltage (ZV). At the end of this interval, $i_{S_T} = i_{S_B} = \frac{i_S}{2}$ and $i_p = 0$. The body diodes of S_2 and S_3 commutes naturally.

3) Mode 3: (Fig. 3c, $t_2 < t < t_3$): At $t = t_2$, the devices S_2 and S_3 start conducting and i_p becomes negative and falls linearly with the same slope. The grid side currents i_{S_T} keeps falling linearly and i_{S_B} keeps rising with same slope as in $Mode\ 2$. At $t = t_3$, i_{S_T} becomes zero and i_{S_B} reaches steady value i_S. The primary current becomes $i_p = -\frac{N_2}{N_1} i_S$.

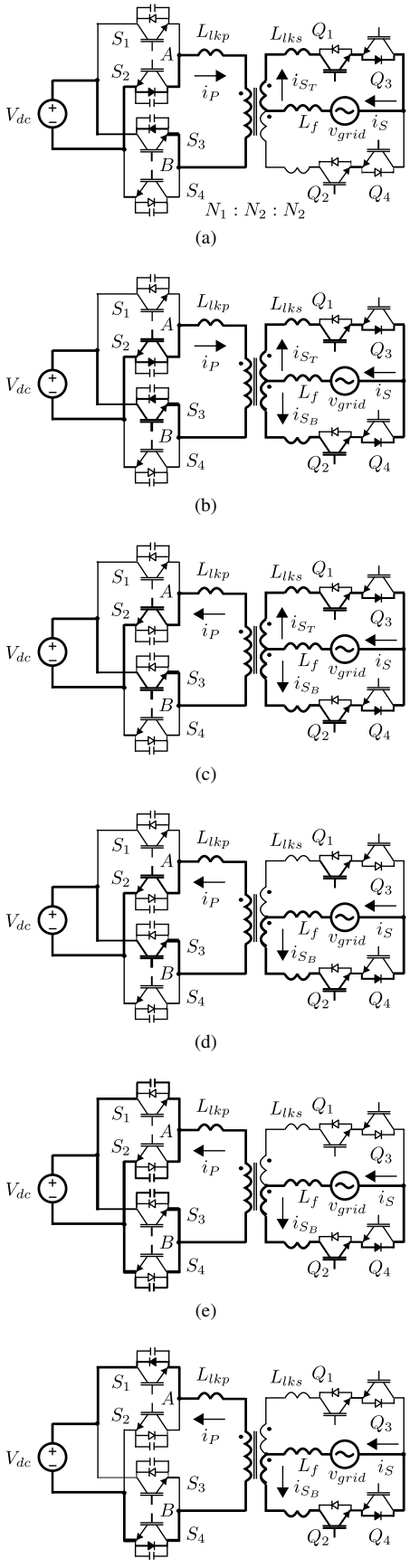


Fig. 3: Commutation process for AC to DC active power flow- (a) $Mode$ 1, (b) $Mode$ 2, (c) $Mode$ 3, (d) $Mode$ 4, (e) $Mode$ 5, (f) $Mode$ 6.

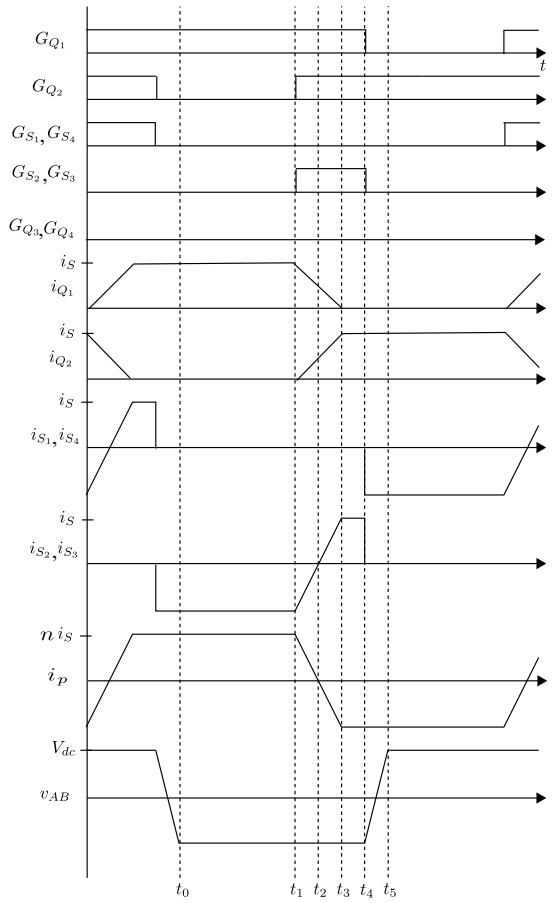


Fig. 4: Switching waveforms illustrating soft-switching operation during AC to DC power flow

4) Mode 4: (Fig. 3d, $t_3 < t < t_4$): At $t = t_3$ when i_{S_T} reaches zero, the body diode of Q_3 is reverse biased. So, i_{S_T} can not be negative and it remains at zero. Q_2 and the anti-parallel body diode of Q_4 keeps conducting and $i_{S_B} = i_S$. In DC side, S_2 and S_3 are conducting i_p, where $i_p = -\frac{N_2}{N_1} i_S$.

5) Mode 5: (Fig. 3e, $t_4 < t < t_5$): At $t = t_4$ the switches S_2, S_3 and Q_1 are turned OFF. The turn OFF of Q_1 is zero current switching (ZCS) as $i_{S_T} = 0$. Considering the parasitic capacitance across the DC side switches, the turn OFF of S_2, S_3 is soft-switched. The circuit equations are given as:

$$v_{C_1} + v_{C_2} = V_{dc} \tag{7}$$

$$v_{C_3} + v_{C_4} = V_{dc} \tag{8}$$

$$C_2 \frac{dv_{C_2}}{dt} = C_1 \frac{dv_{C_1}}{dt} + i_p \tag{9}$$

$$C_3 \frac{dv_{C_3}}{dt} = C_4 \frac{dv_{C_4}}{dt} + i_p \tag{10}$$

where C_1, C_2, C_3, C_4 are the parasitic capacitance across the switches S_1, S_2, S_3, S_4 respectively. The voltages v_{C_1} and v_{C_4} falls linearly with slopes $\frac{ni_S}{C_1+C_2}$ and $\frac{ni_S}{C_3+C_4}$

respectively where $n = \frac{N_2}{N_1}$

$$v_{C_1} = -\frac{ni_S}{C_1 + C_2}t + V_{dc} \tag{11}$$

$$v_{C_4} = -\frac{ni_S}{C_3 + C_4}t + V_{dc} \tag{12}$$

Considering identical devices, device capacitances are of similar order. At $t = t_5$, v_{C_1} and v_{C_4} are discharged to zero. Due to anti-parallel body diodes of S_1 and S_4, the voltages v_{C_1} and v_{C_4} can not be negative. So at $t = t_5$ body diodes of S_1 and S_4 start conducting.

6) Mode 6: (Fig. 3f, $t > t_5$): In this interval, the switch Q_2 and the anti-parallel body diode of Q_4 conduct the current i_S. The body diode of S_1 and S_4 continue to conduct and the power is transferred from AC to DC side.

The above commutation process shows the current is transferred from switch Q_1 to Q_2, and the transformer current polarity is reversed.

B. Active power flow direction: DC to AC

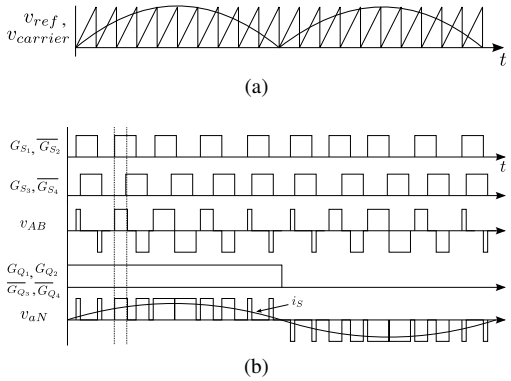


Fig. 5: Modulation strategy for DC to AC active power flow- (a) carrier and reference waveform (b) switching scheme in a line frequency cycle.

In this case, the modulation strategy is employed in the DC side inverter by switching it at high frequency as shown in Fig. 5. The grid side switches are switched at line frequency (Fig. 5). The commutation process and the switching waveforms are shown in Fig. 6 and Fig. 7 respectively. The grid with inductive filter is shown as AC current source. The gating signals of S_1 and S_3 are phase shifted and the phase sift varies sinusoidally over the line cycle. S_2 and S_4 are complementary switched with S_1 and S_3 respectively. The grid side switches Q_1 and Q_2 are kept ON when i_S is positive. When the polarity of i_S is reversed, Q_3 and Q_4 are turned ON and Q_1 and Q_2 are gated OFF. The commutation process is described here for one high frequency half cycle $\frac{1}{T_S}$. In the rest of the cycle the intervals are repeated in same sequence with other symmetrical switches.

1) Mode 1: (Fig. 6a, $t < t_0$): The DC side switches S_1, S_4 and the AC side switch Q_1 and the body diode of Q_3 are conducting to transfer the active power from DC to AC side. Though the switch Q_2 is ON, $i_{S_B} = 0$ as the

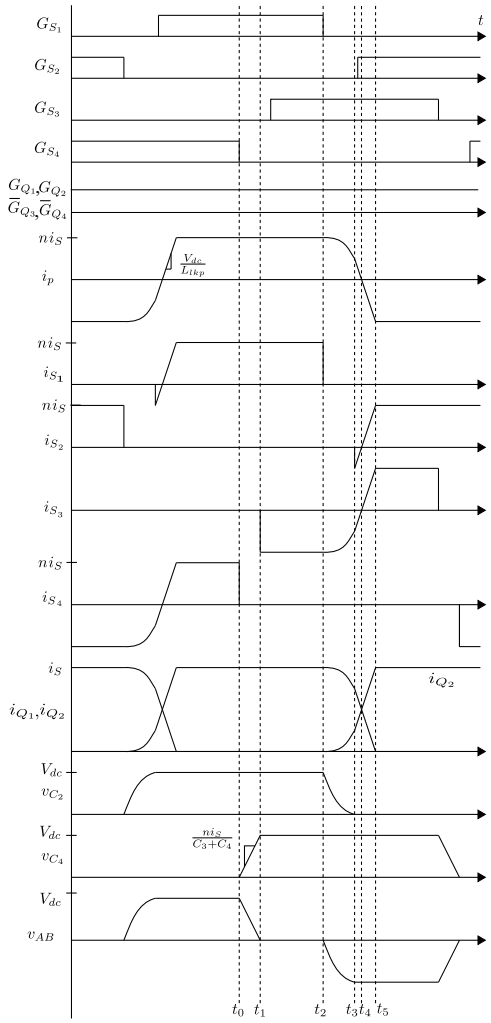


Fig. 7: Switching waveforms illustrating soft-switching operation during DC to AC power flow

body diode of Q_4 is reversed biased. The DC and AC side switch currents are $i_p = ni_S$ and $i_{S_T} = i_S$ respectively. The switches S_2 and S_3 block voltage V_{dc}. The voltage across the switch Q_4 is $2V_{dc}\frac{N_2}{N_1}$.

2) Mode 2: (Fig. 6b, $t_0 < t < t_1$): At $t = t_0$ the switch S_4 is turned OFF. Due to device capacitance the voltage can not immediately rise which ensures the ZVS of S_4. i_p starts discharging the parasitic capacitance C_3 and charging C_4. The governing circuit equations are (8) and -

$$C_4\frac{dv_{C_4}}{dt} = C_3\frac{dv_{C_3}}{dt} + i_p \tag{13}$$

The voltage v_{C_3} falls linearly as given in equation (14).

$$v_{C_3} = -\frac{ni_S}{C_3 + C_4}t + V_{dc} \tag{14}$$

At $t = t_1$, C_3 discharges to zero and the the anti-parallel body diode of S_3 is forward biased.

3) Mode 3: (Fig. 6c, $t_1 < t < t_2$): During this duration, the switch S_1 and the body diode of S_3 are conducting. This mode applies a zero voltage across the high frequency

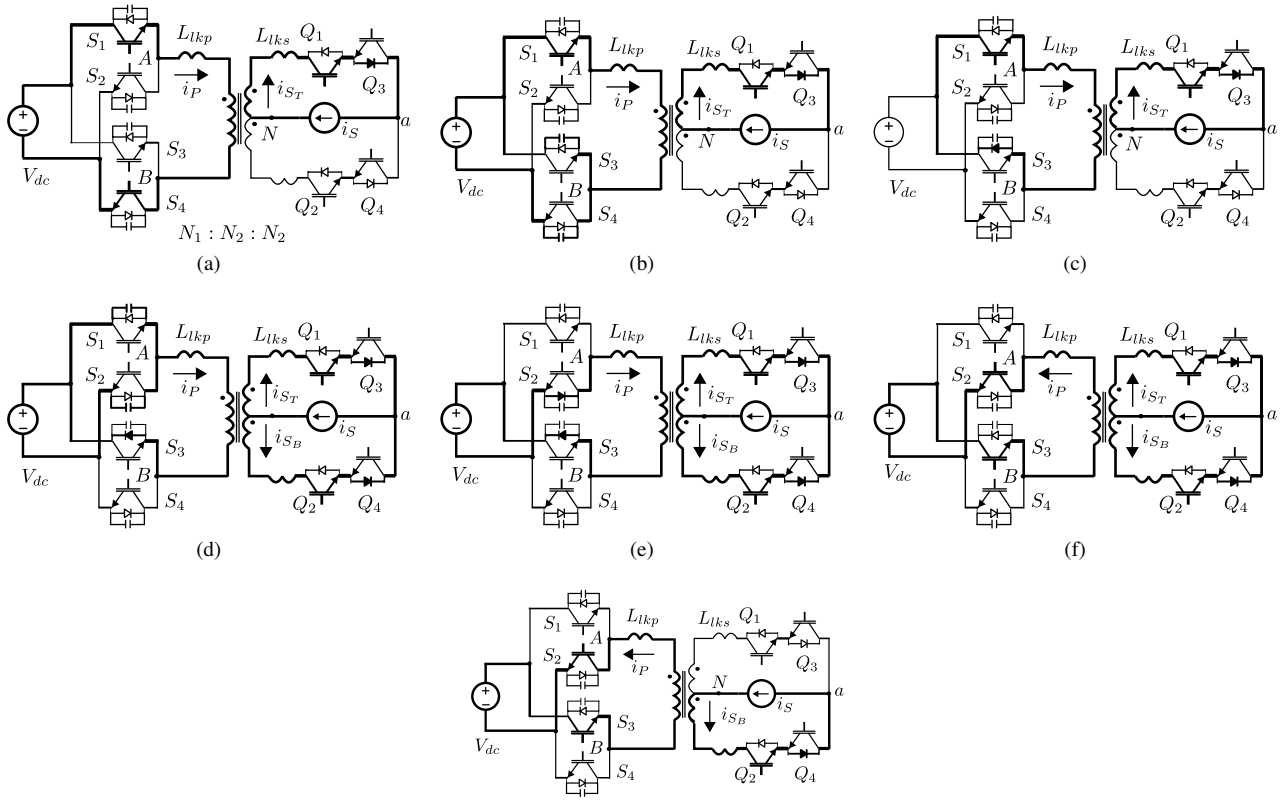


Fig. 6: Commutation process for DC to AC active power flow- (a) $Mode$ 1, (b) $Mode$ 2, (c) $Mode$ 3, (d) $Mode$ 4, (e) $Mode$ 5, (f) $Mode$ 6, (g) $Mode$ 7.

transformer primary. There is no active power transfer during this interval. The secondary side current is free wheeling through Q_1 and body diode of Q_3. The gate pulse of S_3 is applied in this interval to ensure the ZVS turn ON while the body diode is conducting. At the end of this interval S_1 is turned OFF.

4) Mode 4: (Fig. 6d, $t_2 < t < t_3$): i_p starts starts charging and discharging the device capacitances across S_1 and S_2 respectively. A negative voltage is appeared across transformer terminal AB. The negative voltage forward biases the body diode of Q_4. Q_2 and the body diode of Q_4 start conducting. The currents i_p and i_{S_T} start falling in this interval. The governing circuit equations are given in (7) and-

$$C_1 \frac{dv_{C_1}}{dt} = C_2 \frac{dv_{C_2}}{dt} + i_p \tag{15}$$

$$v_{C_1} + L_{lkp} \frac{di_p}{dt} = 0 \tag{16}$$

where L_{lkp} is the transformer leakage inductance seen from DC side. Solving the above equations, the primary current is expressed as-

$$i_p = n i_S \cdot \cos\left(\frac{t}{\sqrt{L_{lkp}(C_1 + C_2)}}\right) \tag{17}$$

The AC side currents i_{S_T} and i_{S_B} are given as-

$$i_{S_T} = \frac{i_S}{2} + \frac{i_S}{2} \cdot \cos\left(\frac{t}{\sqrt{L_{lkp}(C_1 + C_2)}}\right) \tag{18}$$

$$i_{S_B} = \frac{i_S}{2} - \frac{i_S}{2} \cdot \cos\left(\frac{t}{\sqrt{L_{lkp}(C_1 + C_2)}}\right) \tag{19}$$

The voltage across the device S_1 is expressed as-

$$v_{C_1} = n i_S \cdot \sqrt{\frac{L_{lkp}}{(C_1 + C_2)}} \sin\left(\frac{t}{\sqrt{L_{lkp}(C_1 + C_2)}}\right) \tag{20}$$

At $t = t_3$ v_{C_1} reaches V_{dc} and v_{C_2} becomes zero. The body diode of S_2 is forward biased.

5) Mode 5: (Fig. 6e, $t_3 < t < t_4$): In this interval the body diode of S_2 and S_3 are conducting. A negative voltage is applied across L_{lkp} and reduces the current i_p further. The voltage drop across L_{lkp} is given as

$$L_{lkp} \frac{di_p}{dt} + V_{dc} = 0 \tag{21}$$

Solving (21) the primary current i_p -

$$i_p = -\frac{V_{dc}}{L_{lkp}}(t - t_3) + i_p(t_3) \tag{22}$$

In this interval i_{S_T} and i_{S_B} are expressed as-

$$i_{S_T} = \frac{i_S}{2} + \frac{i_p(t_3)}{2n} - \frac{V_{dc}}{2nL_{lkp}}(t - t_3) \tag{23}$$

$$i_{S_B} = \frac{i_S}{2} - \frac{i_p(t_3)}{2n} + \frac{V_{dc}}{2nL_{lkp}}(t - t_3) \tag{24}$$

This interval ends at $t = t_4$ when $i_p = 0$. The AC side current $i_{S_T} = i_{S_B} = \frac{i_S}{2}$. The gating signal of S_2 is applied within this interval to achieve ZVS turn ON, when the body diode is conducting. The condition to achieve ZVS turn ON is given as-

$$ni_S \cdot \sqrt{\frac{L_{lkp}}{C_1 + C_2}} > V_{dc} \tag{25}$$

6) Mode 6: (Fig. 6f, $t_4 < t < t_5$): In this interval i_p becomes negative and continues to fall with same slope $-\frac{V_{dc}}{L_{lkp}}$. i_{S_T} and i_{S_B} keep falling and rising respectively with same slope as in last interval. The devices S_2 and S_3 start conducting. At $t = t_5$, i_p reaches to ni_S and $i_{S_B} = i_S$ and $i_{S_T} = 0$.

7) Mode 7: (Fig. 6g, $t > t_5$): In this interval S_2,S_3, Q_2 and body diode of Q_4 are conducting to transfer the active power from DC to AC side.

In the above discussion, current is transferred from switch S_1, S_4, Q_1 to S_2, S_3, Q_2 and the transformer current polarity is reversed.

III. Simulation results

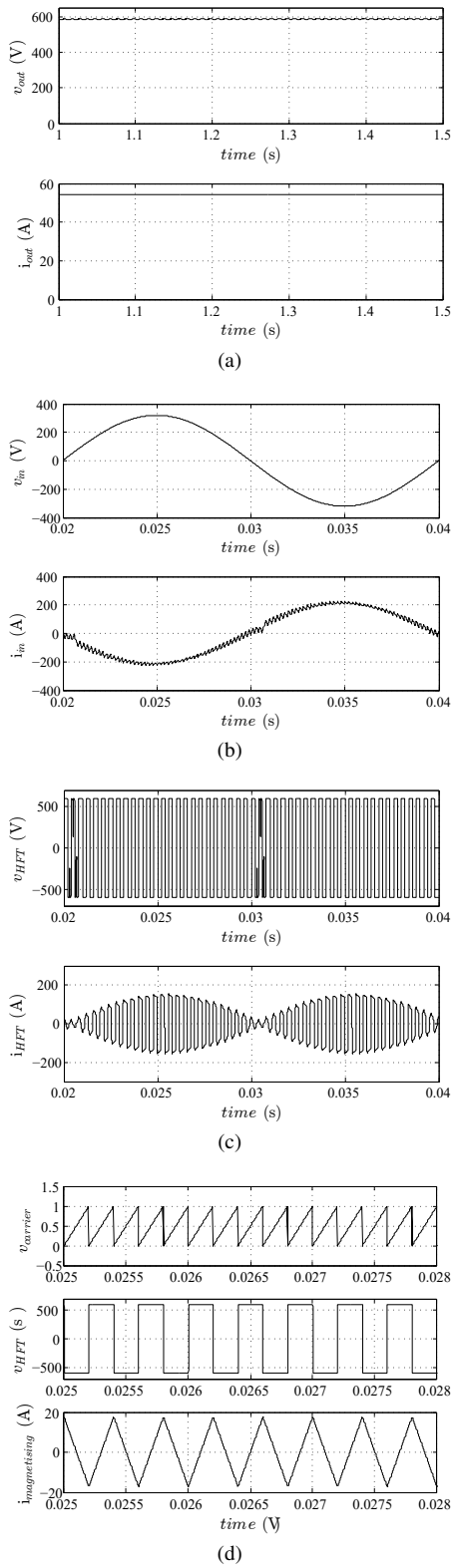
The proposed topology is simulated for both the direction of power flow. The simulation results are verified with theoretical analysis. The open loop simulation parameters are presented in Table I.

TABLE I: Simulation Parameters

Parameter	Value
AC RMS voltage (V)	230
DC bus voltage (V)	600
Line frequency $f(Hz)$	50
Carrier frequency (AC to DC power flow)	5 kHz
Carrier frequency (DC to AC power flow)	10 kHz
Power (kW)	$\pm$33.3
HFT turns ratio ($N_1 : N_2 : N_2$)	25:17:17
Filter inductance (at 50 Hz) (AC to DC power flow)	$960\mu H$
Filter inductance (at 50 Hz) (DC to AC power flow)	$255\mu H$
HFT leakage impedance (from DC side)	$5.5\mu H$
Capacitance across the DC side switches	40 nF
Peak modulation index(M) (DC to AC power flow)	0.8
Dead time of HF inverter (DC to AC power flow)	$1\mu S$

A. Simulation results for AC to DC side power flow

The simulated output voltage and current waveforms are shown in Fig. 8a. The output voltage and current are 600 V and 55.56 A respectively. The input voltage and current waveform are shown in Fig. 8b. HFT output voltage and current is shown in Fig. 8c. The flux balance waveform of the HFT is shown in Fig. 8d. Fig. 9 shows the ZCS of Q_1 and Q_2 as well as ZVS of $S_{1,4}$ and $S_{2,3}$.



(a) (b) (c) (d)

Fig. 8: Simulated waveform for AC to DC active power flow- (a) output voltage and current (b) input voltage and current (c) HF transformer voltage and current (d) HFT flux balance.

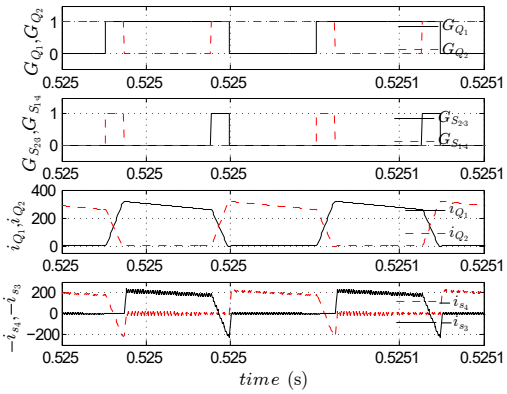


Fig. 9: Soft-switching waveforms for AC to DC active power flow

B. Simulation results for DC to AC side power flow

The simulated output voltage (v_{out}) and current (i_{out}) are in phase as in Fig. 10a. The peak values of output voltage and current are 320 V and 198 A respectively. The output voltage and current of the converter before the filter contain switching ripple. The input voltage of the HFT (v_{AB}) and input current (i_p) are shown in Fig. 10b. The flux balance atthe HFT is shown in Fig. 10c. The average primary voltage and average magnetising current are zero over a switching cycle. The zero voltage switching waveforms of DC side switches are shown in Fig. 10d.

IV. Conclusion

In this paper a high frequency link DC to AC converter topology along with modulation strategies for bidirectional power flow has been proposed. The topology with proposed control strategy has following advantages- (a) single stage bidirectional power flow, (b) soft-switching for both direction of power flow without using additional snubber circuit; (c) for AC to DC side power flow, ZCS ON-OFF of AC side switches and ZVS ON-OFF of DC side switches have been achieved, and also the AC side switches are switching half of the line frequency cycle; (d) for DC to AC side power flow, AC side switches are line frequency switched and the DC side switches are ZVS ON-OFF (e) galvanic isolation using high frequency transformer helps to achieve low volume high power density of the converter. The soft-switching operation of the converter has been analysed in detail. The presented simulation results verify the operation of the converter. This can be promising solution for the applications like- UPS system, vehicle to grid (V2G) integration, battery based energy storage system.

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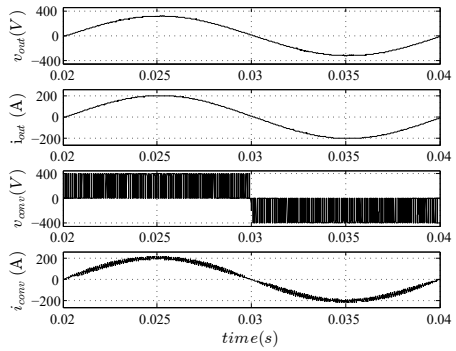
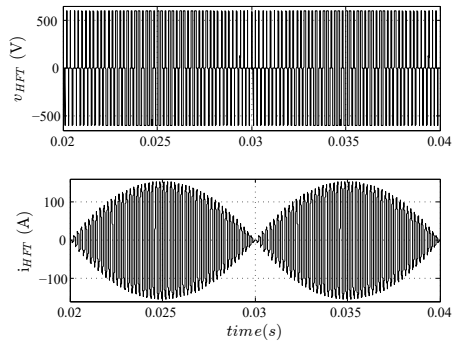


(a)



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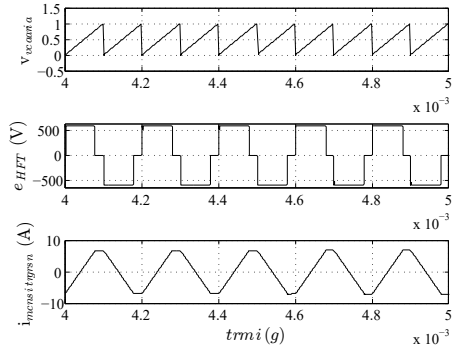
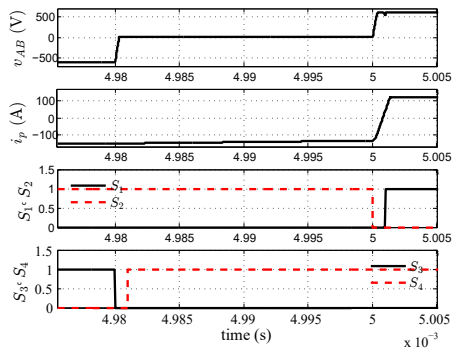


(c)



(d)

Fig. 10: Simulated waveform for DC to AC active power flow- (a) voltage and current waveforms before and after the output filter (b) HF transformer voltage and current (d) HFT flux balance (e) soft-switching waveforms.

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